REMARKS

Reconsideration and further examination are respectfully requested. Claims 1-18 are currently pending.

Rejections under 35 U.S.C. §112, second paragraph

Claims 11-14 were rejected to under 35 U.S.C. §112, second paragraph for various informalities. Applicants have amended the claims to fix the informalities identified by the Examiner. Accordingly, Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

Rejections under 35 U.S.C. §103

Claims 1 and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Munson et al (hereinafter Munson), U.S. 20010037444, in view of "The RISC Concept – A survery of Implementations", Esponda et al., (hereinafter Esponda), September 1991.

Munson:

Munson describes an instruction processing system for processing branch instructions and fetching instructions from an instruction memory. Munson describes, at paragraph 007:

"... In order for a pipelined microprocessor to operate efficiently, an instruction fetch unit at the head of the pipeline must continually provide the pipeline with a stream of microprocessor instructions. However, conditional branch instructions within an instruction stream prevent the instruction fetch unit from fetching subsequent instructions until the branch condition is fully resolved. In pipelined microprocessor, the branch condition will not be fully resolved until the branch instruction reaches an instruction execution stage near the end of the microprocessor

pipeline. Accordingly, the instruction unit will stall because the unresolved branch condition prevents the instruction fetch unit from knowing which instructions to fetch next..."

Thus, Munson describes a conditional branch instruction where there is a dependency between two different instruction threads, and where the processing is often delayed based on a resolution of the dependency. Munson describes, in its' specification, various ways in which the dependencies are predicted to reduce delays, for example through the use of branch prediction techniques (paragraph 0029). In the Abstract, Munson states "... If a branch instruction is predicted taken, a block of instructions beginning at the jump target address is fetched and stored in an instruction queue directly following the branch instruction so that multiple streams of instructions are stored in the instruction queue..."

Esponda

Esponda describes the basic concepts of the Reduced Instruction Set Computer (RISC) architectures. Esponda states, at page 5, lines 5-11:

"... In real systems there are many reasons for the regular pipeline flow to be interrupted systematically. The penalty for these disruptions is paid in the form of lost or stall pipeline cycles. The effective parallelism exploited by traditional CISC microprocessors .... is rarely larger than the factor 2, and more likely to be near the factor 1.5. This means that old CISC microprocessors offer very limited form of pipeline parallelism...The main different between RISC and CISC is that the instruction set of the first kind of processors was explicitly designed to allow the sustained execution of instructions in one cycle as average..."

The Examiner states, at pages 4-5 of the office action:

"... Munson does not explicitly teach: executing the first instruction in a first stage of a processing pipeline... and forwarding the first instruction to a next stage of the processing pipeline while forwarding the second instruction to the first stage of the processing pipeline such that the first instruction and the second instruction can be executed simultaneously in the processing pipeline...However, Esponda teaches executing a first instruction in a first stage of a processing pipeline .... first instruction being *instruction i,* and first stage being *instruction fetch,*) and forwarding the first instruction to a next stage of the processing while forwarding the second

instruction to the first stage of the processing pipeline such that the first instruction and second instruction can be executed simultaneously in the processing pipeline... It would have been obvious to a person of ordinary skill in the art ... to combine the teachings of Munson and Esponda because teaching of Esponda include multiple stages within a pipeline achieving parallel execution of instruction threads would improve the efficiency of Munson by allowing for execution of instruction by a factor of three (Esponda, pg. 5, lines 1-5)..."

Examiner has failed to establish a prima facie case of obviousness

As stated in M.P.E.P. §2143, "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

1. No motivation for the modification suggested by the Examiner

It is well established that "...If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)

Munson describes a branch prediction mechanism, which is part of, and intended for use, in a Complex Instruction Set Computer (CISC). In such a computer, as described by Esponda "... In real systems there are many reasons for the regular pipeline to be interrupted systematically". Once such instance is as a result of a branch calculation, when the flow of instructions is changed. To overcome this problem, Munson has developed a branch prediction mechanism, which allows for pre-fetching of the expected branch path microcode.

Esponda, in contrast, teaches about RISC systems, where "the instruction set ... was explicitly designed to allow the sustained execution of instructions in one cycle as average..." With regard to branching, Esponda states, at page 7, paragraph (f):

"... The most complex hazard menacing the uninterrupted pipeline flow is branching. Instructions are fetched sequentially but a taken branch can alter the flow of instructions. After a taken branch a new instruction located at the branch target has to be fetched and the pipeline flushed of now irrelevant instructions.... This amounts to many lost pipeline cycles in typical CISC processors, which flush the pipeline after each taken branch... RISC processors use other strategies. First ... the branching decision is make very early in the execution path – possibly in the decode stage. This can be done only if the branching condition tests are very simple, like for example a register compare to zero or a condition flag test. At the end of the decode phase the processor can start fetching instructions from the new target...In this case the branch is a delayed branch..."

The combination of Esponda with Munson would be an attempt to force elements of a RISC architecture into a particular solution for branching for a CISC architecture. Such a combination would render the prior art being modified unsatisfactory for its intended purpose of "processing branch instructions ..."(Munson, Abstract). For at least this reason, there is no proper motivation for the modification suggested by the Examiner, and the rejection should be withdrawn.

2. There is no reasonable expectation of success in the combination of Munson and Esponda

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)" The proposed modification of Munson, i.e., to change the architecture from a CISC architecture to a RISC architecture, would change the overall principle and purpose of Munson, which is to provide a solution to branching delays in a CISC processor. For at least the

reason that the proposed modification would change the principle of operation of the prior art being modified, there is no reasonable expectation of success arising from the combination. Thus, the combination fails to meet the burden required to establish a prima facie case of obviousness, and the rejection should be withdrawn.

3. Combination neither describes nor suggests the claimed invention

Both Esponda and Munson deal with sequential instructions in a stream; Munson arguable changes the individual threads of the instructions in response to a branch result, but the instruction threads are still dependent upon each other. Applicants' claims, as amended, clearly distinguish the claimed invention over that of Munson and Esponda, by clarifying that the instruction threads are 'independent'. As described in Applicants specification at page 13 "the state of each thread is independent of the state of all others..." Applicants have replaced claim 17 to clearly recite a claim towards threads which have different register sets; thus, there is no dependencies between the instruction threads as they await utilization of shared resources. Accordingly, for at least the reason that neither Munson, Esponda or the combination thereof describe or suggest the parallel processing of 'independent instruction threads' as recited in independent claims 1 and 5, the claims are patentably distinct over the combination of references, and the rejection should be withdrawn.

Claims 2-4 and 6-18:

Claims 2-4 and 6-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Munson, Esponda as applied to claims 1 and 5 above, and further in view of Epps et al. (hereinafter Epps) U.S. 6,813,243.

Epps:

Epps describes, in the Abstract: "...A pipelined linecard architecture for receiving, modifying, switching, buffering, queuing and dequeuing packets for transmission in a communications network. The linecard has two paths: the receive path, which carries packets into the switch device from the network, and the transmit path, which carries packets from the switch to the network...."

Applicants note that claims 2-4 and claims 6-18 serve to further depend upon, and add patentable limitations to, independent claims 1 and 5. Applicants have described above why independent claims 1 and 5 are believed to be non-obvious over the cited art. Epps, although it describes independent transmit and receive paths, fails to overcome the inadequacies cited above in the combination of Esponda and Munson. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Although dependent claims 2-4 and 6-18 serve to add further patentable limitations to their parent independent claims, they are patentable for at least the same reasons as their parent claims, and it is respectfully requested therefore that this rejection be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at the number listed below so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

2/21/2006
Date

Lindsay G. McGuinness, Reg. No. 38,549
Attorney/Agent for Applicant(s)
McGuinness & Manaras LLP
125 Nagog Park
Acton, MA 01720
(978) 264-6664

Docket No. 120-100
Dd: 2/21/06